REMARKS

Claims 1-8 are pending in the present application.

I. FORMAL MATTERS

Applicant notes with appreciation that the Final Office Action again acknowledges the claim to foreign priority under 35 U.S.C. § 119(a)-(d) or (f) and indicates that the certified copies of the priority documents have been received.

Applicant notes with appreciation that the Final Office Action indicates that the drawings filed on July 24, 2001 are acceptable, as requested in the Amendment filed on April 28, 2004.

Applicant notes with appreciation that the Office Action includes a copy of the PTO Form 1449 that was submitted with the Information Disclosure Statement filed on July 24, 2001, as requested in the Amendment filed on April 28, 2004.

II. PRIOR ART REJECTION

Claims 1-8 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over U.S. Patent No. 6,025,822 (Motegi, et al.). The examiner's rationale is substantially

similar to the rejection presented in the previous Office Action dated January 28, 2004. This rejection is traversed.

In response to Applicant's argument that the column drivers 21 of Motegi are not connected in series, the Examiner asserts that the column drivers 21 are arranged in parallel, but are connected in series. Applicant submits that Fig. 7 of Motegi shows four (4) column drivers 21 clearly connected in parallel. Clearly, the column drivers 21 shown in Fig. 7 of Motegi are connected in parallel.

In response to Applicant's argument that Motegi does not disclose a selection section for selecting one of a signal in synchronization with the timing signal and the control data signal input to the data input section, or a data output section for outputting the selected signal to the data input section of a second column electrode driving circuit, the Examiner asserts that Fig. 8 of Motegi teaches a selector 34 that inherently works in synchronization with the timing signal and control data signal input to the data input section corresponding to the selection section. Regarding the claimed data output section, the Examiner asserts that the memory unit 10 corresponds to this claim element.

The selector 34 of Motegi is part of the preferred embodiment shown in Fig. 1, and the memory unit 10 is part of the conventional driving circuit shown in Fig. 8. Applicant submits that the memory unit 10 of Fig. 8 does not output the signal selected by the selector 34 because these elements are part of completely different circuits (preferred embodiment and prior art). Therefore, Applicant submits that the

Examiner's rejection is improper. Column 9, lines 47-51 of Motegi teach that the column drivers 101-110 function as the display, RAM 24, the data selector 34, the memories 35a-35n, etc., of the conventional driving circuit of Fig. 8. However, Applicant submits that this description does not adequately relate the functions of the memory and the selector and teach that the memories 36a-36n output signals selected by the data selector 34, as required by claim 1. Further, Applicant submits that the Examiner does not indicate any section of the specification of Motegi that allegedly teaches that the data selector 34 and the memory unit 10 perform these functions of the claimed selection section and data output section. Fig. 8 of Motegi shows the memories 36a – 36n arranged adjacent to the data selector 34. The data selector 34 of Motegi is described as "distributing the data of 7 lines . . . to the memories 35a – 35n" (see column 3, lines 12 – 20). Therefore the data selector 34 of Motegi, et al. performs a very different function than the presently claimed selector section. Specifically the data selector 34 of Motegi, et al. is merely used to "split" up the incoming RGB signals into the appropriate memory for further processing. Therefore, Applicant submits that Motegi does not teach or suggest the selection section of claim 1.

In response to the argument presented in the amendment filed on April 28, 2004 that the controller 2 shown in Fig. 6 of Motegi does not show a timing signal that is supplied on the specific path defined by claim 6, the Examiner asserts that the controller 23 of Motegi may not show a timing signal, but it is inherent. Applicant submits that the function of the controller 23 of Motegi is substantially different than the claimed invention. Therefore, the path of the timing signal that is defined in claims 6 and 7 is not taught or suggested anywhere in Motegi and would certainly not

be inherent in the design of controller 23 as the Examiner suggests, since the circuit is of a very different design.

Further, Applicant submits that Motegi does not teach or suggest a timing signal that is output from a first column electrode driving circuit and supplied to a first row electrode driving circuit sequentially through a circuit board so as not to be crossed with a signal circuit, as recited by claim 8. The Examiner did not respond to this argument in the present office action.

Also, in the rejection of claim 6, the examiner relies on Fig. 7 and Fig. 1. Fig. 1 shows an embodiment of the invention. Fig. 7 shows a prior art LCD. The Examiner has not asserted reasons why it would have been obvious to combine features of the prior art LCD with the invention.

Therefore, based on the foregoing, Applicant submits that the Examiner has not formed a prima facie case of obviousness.

Applicant invites the Examiner to contact the undersigned at the telephone number listed below if the Examiner believes that a telephone interview would expedite prosecution of the present application.

Applicant believes that no additional fees are due for the subject application. However, if for any reason a fee is required, a fee paid is inadequate or credit is owed for any excess fee paid, you are hereby authorized and requested to charge Deposit Account No. **04-1105**.

Respectfully submitted,

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Customer No.: 21874

John J. Penny, Jr.
Reg. No. 36,984
Intellectual Property Practice Group of
EDWARDS & ANGELL, LLP
P. O. Box 55874
Boston, MA 02205
Tel: (617) 517-5549
Fax: (617) 439-4170

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